IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicants	: Sydir et al.	Art Unit	: 2434
Serial No.	: 10/749,913	Examiner	: Farid Homayounmehr
Filed	: December 29, 2003	Assignee	: Intel Corporation
Confirm. No.:	1409		

Title : NETWORK PROCESSOR HAVING CRYPTOGRAPHIC PROCESSING INCLUDING AN AUTHENTICATION BUFFER

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PRE-APPEAL BRIEF REQUEST FOR REVIEW

Applicants request review of the final rejection in the above-identified application. No amendments are being filed with this request. This request is being filed with a Notice of Appeal.

Claims 42, 44, 45, 48 to 53, 55, 56, 58, 60, 62, 63, 65 to 70 and 72 to 77 are rejected under 35 U.S.C. § 103(a) as being obvious over Ohta et al. (U.S. Patent Application Publication Number 2002/0083317 hereinafter "Ohta") in view of Tardo et al. (U.S. Patent Number 7,082,534). Claims 46, 47 and 54 and 61 are rejected under 35 U.S.C. § 103(a) as being obvious over Ohta in view of Tardo and in further view of Corder et al. (U.S. Patent Number 7,069,447). Claims 43, 57, 59, 64 and 71 are rejected under 35 U.S.C. § 103(a) as being obvious over Ohta in view of Tardo and in further view of Yoaz et al. ("Speculation Techniques for Improving Load related Instruction Scheduling" hereinafter "Yoaz")

Applicants respectfully submit that the Examiner has committed clear errors in the rejection by improperly identifying essential elements needed to establish a *prima facie* obviousness rejection, at least for the reasons described in sections A-C, any one of which is cause to withdraw the rejection.

A. The Examiner has improperly indicated that the cited art teaches the claim limitation of "one of the authentication cores processes data in 16-byte blocks and another one of the authentication cores processes data in 64-byte blocks," of independent claims 58 and 68.

The Examiner has indicated that Ohta teaches this limitation at paragraph [0016] (see pages 8 of the Office Action), which states

> Here, in the above-mentioned security communication packet processing apparatus, the data block for the encryption processing can be 64 bits, and the data block for the authentication processing can be 512 bits. In this case, the data block accumulation unit may output the data blocks when it accumulates eight encrypted data blocks (paragraph [0016] of Ohta).

However, Ohta mentions nothing about two authentication cores because Ohta only teaches a single authentication core. Furthermore, the Examiner's statement that "outputting blocks of data to the encryption and authentication processors in multiples of 8 bits, which include all processing block in claims 8 and 9" (see pages 8 of the Office Action) is confusing since 8 bits is not even mentioned in the cited passage much less the claim. In response to Applicants' arguments, the Examiner incorrectly stated that

> "as admitted by the Applicant, paragraph [0016] teaches that the data block for encryption processing can be 64 bits, which is clearly a multiple of 8 bits (one-byte). The claim requirement is 16 bytes and 64 bytes, which are clearly multiples of one byte" (see page 4 of the Office Action).

However, the Examiner statement is incorrect because Applicants' made no such admissions nor has the Examiner cited the claim limitation correctly. The claim cites one of the authentication cores processes data in 16-byte blocks and another one of the authentication cores processes data in 64-byte blocks. The Examiner's rational that 16-byte blocks and 64-byte blocks are multiples of 8 bits or 1 byte seems irrelevant or at least does not logically support an argument that Ohta teaches

authentication cores processing data in 16-byte blocks, for example. Moreover, Applicants respectfully submit that the cited passage of Ohta (paragraph [0016]) clearly and only states 512 bits for authentication processing which, even assuming 8 bits per byte, is just 64-byte blocks. Thus, there is not even a teaching that suggests authentication of the recited 16-byte blocks in the cited Ohta passage. Thus, the Examiner has committed clear error by not identifying the claim element in the cited art nor has he accounted for the gap between the cited art and the claimed invention.

B. The Examiner has improperly indicated that the cited art teaches the claim limitation of "one of the cipher cores processes data in 8-byte blocks and another one of the cipher cores processes data in 16-byte blocks," of independent claims 52 and 68.

The Examiner has indicated that Ohta teaches this limitation at paragraph [0016] (see page 9 of the Office Action). However, Ohta mentions nothing about two cipher cores because Ohta only teaches a single cipher core. Furthermore, the Examiner's statement that "outputting blocks of data to the encryption and authentication processors in multiples of 8 bits, which include all processing block in claims 44 and 45" (see page 9 of the Office Action) is confusing since the cited passage mentions nothing about 8 bits nor is the Examiner's statement rationally related to the recited claims. Moreover, Applicants respectfully submit that the cited passage clearly and only states 64-bit data blocks for encryption processing which, assuming 8 bits per byte, is 8-byte blocks. Thus, there is not a teaching that suggests encryption of 16-byte blocks in the cited passage. The Examiner relies on his rationale with respect to claims 52 and 68 that 16 bytes is a multiple of 8-bits (see pages 4 and 5 of the office Action). If so, as stated in section A, this argument also seems irrelevant or at least does not logically support an argument that Ohta teaches cipher cores processing data in 16-byte blocks,

for example. Thus, the Examiner has committed clear error by not identifying the claim element in the cited art nor has he accounted for the gaps between the cited art and the claimed invention.

C. The Examiner has improperly indicated that the cited art teaches the claim limitation of "the authentication buffer connected to the cipher core and comprising buffer elements, each buffer element storing data corresponding to a respective one of the processing contexts and having a size that is at least as large as a largest authentication algorithm block size implemented by the authentication cores," of independent claims 42, 52, 58, 63, 68 and 72.

The Examiner has indicated that Ohta teaches the limitation at paragraph [0011] citing "a data block accumulation unit that outputs the accumulated amount to the authentication processing unit when it reaches the smallest data block size for the authenticating processing" (emphasis added, see page 8 of the Office Action). The Examiner also points to FIGS. 1 and 2 of Ohta and their associated text as further support and stating that "(i)t would be only logical to have a buffer size that is large enough to accommodate the largest block size" (see page 8 of the Office Action). However, Ohta only describes a single authentication core in FIGS. 1 and 2 and therefore Ohta does not teach more than one authentication core much less authentication cores requiring a different authentication algorithm block size. Therefore, Ohta does not teach that each buffer element has a size that is at least as large as a largest authentication algorithm block size implemented by the authentication cores.

Tardo merely mentions different authentication algorithms. Tardo does not teach buffer elements much less a buffer element having a size that is at least as large as a largest authentication algorithm block size implemented by the authentication cores.

Accordingly, for at least the reasons indicated above, even if Tardo were combined with Ohta, the resulting hypothetical combination would not disclose or suggest that each buffer element has a size that is at least as large as a largest authentication algorithm block size implemented by the authentication cores. For example, even using Tardo's authentication cores and assuming more than one authentication core have different block sizes, Ohta clearly says that when the smallest data block size is achieved the data block it is outputted and not the largest authentication algorithm block size implemented by the authentication cores (see paragraph [0011] of Ohta). Even the Examiner's response to Applicants' arguments fails to logically account for the gap between the cited art and the claimed invention (see pages 2 and 3 of the Office Action).

In view of the above, it is submitted that there are clear errors in this rejection. Accordingly, Applicants respectfully request that the art rejection be withdrawn.

No fee is believed to be due for this Pre-Appeal Brief Request for Review; however, if any other fees are due, please apply such fees to Deposit Account No. 50-0845 referencing Attorney Docket: INTEL-013PUS.

I am an attorney acting under 37 CFR §1.34.

Respectfully submitted,

Date: 12 July 2010

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